GENERAL REMARKS

With the amendment above, Applicant has amended the claims to clearly reflect several important features of the claimed invention: that the multiplier is intended for use in computing weighted inputs in signal processing transforms that use sums of weighted inputs; that ability or inability of a multiplier of the invention to compute a product of a given pair of inputs is not determined by multiplier controls such as "halt" controls, but rather by processing structures with reduced capability; and that multipliers of the invention are neither general multipliers with no restrictions on either input or constant multipliers with one input restricted to being a constant and no restrictions on the other input, but rather non-constant and non-general multipliers with restrictions (but not so far as requiring a constant) on at least one input or with restrictions on both inputs.

The Objection to the Specification - Drawings

The Office Action requested a drawing under 37 CFR 1.81.

Applicant has prepared and included Figure 1 showing a non-constant, non-general multiplier according to the present invention. The drawing elements in Figure 1 are all illustrative of material previously described in the original specification and claims. Applicant has amended specification to include appropriate references to the presence of Figure 1, a number label list, and connection between labels in the figure and previously-used terms.

The Objection to Informalities in the Claims

The Office Action objected to claims 1, 9, 10, 13, 17, 25, 26, and 29, requesting delineation of each index limitation with a semi-colon (";") or, between the penultimate and final sections, a semi-colon followed by an and ("; and").

Applicant has amended these claims accordingly. In some of the claims Applicant used enumeration for delineation recursively (in other words parts a, b, and c with part b having parts i, ii, and iii) so Applicant has applied requested semi-colon delineation recursively as well.

The Office Action further objected to claims 6 and 22, advising replacement of original term "the negative" (page 27 line 2 for claim 6) with "a complement".

For both claims 6 and 22, Applicant distinguishes between the value of a number (such as "zero", "pi/3", or "7") and the representation of a number (such as with a binary string in twos' complement, or a two-element hexadecimal representation, or a three digit number). Consequently "the negative" of a number is not the same as "a complement" of a number unless negation is accomplished simply by complementing, which itself presumes some form of binary representation. Applicant notes that in the popular twos' complement representation system, negation is accomplished by complementing followed by addition of the twos' complement representation of the number +1, so that complementing of representation elements (bits) is not the same as negation of a number value.

Applicant wishes to keep reference to number value rather than number representation, and has revised the wording of claims 6 and 22 to reflect this while attempting to avoid informality.

Accordingly, Applicant requests withdrawal of objections on grounds of informality to claims 1, 6, 9, 10, 13, 17, 25, 26, and 29.

The Rejections of Claims Under 35 USC SS 112

Indefinite Language in Claims 1, 13, and their dependent claims

The Office Action rejected claims 1, 2-10, 12-16, 17, 18-26, and 28-32 under 35 USC 112 second paragraph for being indefinite, particularly due to the presence of "can" (line 9, claim 1) and "cannot" (line 13, claim 1) which were not properly described in the claims and interpreted as "would" and "would not" for purposes of examination. Similar language appeared in claim 17, and so both claims 1 and 17 and all their dependent claims were rejected.

Applicant has replaced the indefinite terms "can" and "cannot" in independent claims 1 and 17, and in all their dependent claims, with language that specifies relations between multiplier input values and multiplier output values subject to multiplier control signal states. That a multiplier "can" compute the product of input number X and input number Y means there is at least one multiplier control signal state vector for which, with input numbers X and Y as multiplier inputs, the multiplier output Z is equal to the product X times Y, or XY. That a multiplier "cannot" compute the product of input number X and input number Y means that there is no control signal state vector for which, with input numbers X and Y as multiplier inputs, the multiplier output Z is equal to the product X times Y, or XY.

Applicant's particular intent is to differentiate between fully able general multipliers and reduced-ability non-general multipliers. By reducing the required capabilities below those of a general multiplier, cost savings are possible in such forms as reduced circuit size, complexity, computation time, and power consumption.

It is of course possible to design reduced-ability non-general multipliers that are larger, more complexity, slower, and more power-hungry than fully able general multipliers, but such designs are not useful unless they are superior according to some additional metric such as radiation-hardening.

Applicant notes in Figure 5 of Richardson's US patent 5,262,973 there is disclosed a first multiplier (the entire block diagram) consisting of a second multiplier (block 500) and bypass circuitry. The first multiplier and the corresponding discussion in the specification of the patent do not mention ability or inability to compute products. The main idea of the system in Figure 5, though, is that whenever a multiplier input is 0, +1, or -1 to provide a 0 output directly, the other input directly, or the negative of the other input directly, whereas in all other cases the second multiplier (block 500) computes the product of the multiplier inputs. This saves the cost of running the second multiplier when a multiplier input is 0, +1, or -1, which, according to Figures 1 and 2 of US 5,262,973 may be quite often.

The second multiplier in Figure 5 and the corresponding discussion in the specification similarly make no statement about the ability or inability of the second multiplier to compute products except for the presence of a "halt" control line. With the "halt" control line "on", the second multiplier is disabled. This disabling differs from Applicant's intended meaning of a multiplier that "cannot" compute a product. Applicant submits that the claim language change described above clearly defines the scope of the present invention and differentiates it from multipliers whose computation ability or lack thereof depend on "halt" signals.

Accordingly, Applicant requests withdrawal of rejections of claims 1, 2-10, 12-16, 17, 18-26, and 28-32 under 35 U.S.C. 112 paragraph 2.

Lack of clear definition of "constant multiplier" and "general multiplier" in claims 11 and 27

Office Amendment rejected claims 11 and 27 under 35 U.S.C. 112 sixth paragraph on grounds of terms "constant multiplier" and "general multiplier" (in claim 11 on lines 5-6) preceding "means" without adequate definition of what "constant multiplier means" and "general multiplier means" are.

In the original Specification, Applicant discussed "general multiplier" in the first full paragraph of page 2, and "constant multiplier" in the third full paragraph of page 2. "General multiplier" was also discussed in paragraph 3 on page 8, and "constant multiplier" in paragraph 4 on page 8 and on page 9. However, Applicant did not include formal definition within claims 11 and 27.

Applicant has removed the "whereby" clauses in which the unclear terms appeared in claims 11 and 27, and requests withdrawal of rejections of claims 11 and 27 under 35 U.S.C. 112 sixth paragraph.

The Rejections of Claims Under 35 USC SS 102

The Office Action rejected claims 1-8, 10, 12-24, 26, and 28-32 under USC 102(b) as being anticipated by prior art, citing US Patent 5,262,973 of Richardson and particularly Figure 5 of this prior art.

As above, Applicant will address Figure 5 of US Patent 5,262,973 in two parts: as a first multiplier which is the entire block diagram of Figure 5, and as a second multiplier which is block 500 of Figure 5.

Re Claim 1, page 4 of Office Action

With regard to the paragraph beginning "Re claim 1" on page 4 of the Office Action, Applicant has amended claim 1 to clarify that membership of the "first multiplier-defined restricted set" depends on there being at least one state vector of multiplier control signals such that a mathematically correct product is calculated.

In other words, suppose X and Y are multiplier inputs, and Z is the multiplier output, with X being in 16-bit two's complement, Y being an 18-bit two's complement, and Z being in 34-bit two's complement. For a given Y having a non-zero value, X is a member of a "first restricted set" if and only if there is some set of multiplier control signal values such that Z = X Y. The "first unrestricted set" is clearly "the set of all numbers represented in 16-bit two's complement" in this example, while the "first multiplier-defined restricted set does not include all members of [the] first unrestricted set". So there is at least one possible multiplier input X (in 16-bit two's complement) for which there is no state of control signals such that the multiplier output Z = X Y for the given Y.

Referring to Figure 5, there is no indication in the diagram or the accompanying discussion of the first multiplier (the whole figure) that there are some valid input representations for input X (from block 640) or input Y (from block 650) such that the output Z (block 670) is not the representation of the product X Y. Similarly, the second multiplier (block 500) is presented as a block with "Z = X * Y" in it, but no elaboration. Block 500 could be one of any number of prior art multipliers, or a multiplier according to the present invention could be used as block 500. There is no indication that with X = 1 and some Y, the output of block 500 would not be Y if the "halt" signal were set to allow block 500 to operate when X = 1. In an actual design, a circuit designer would probably pull a general multiplier cell from a standard library (software or a hardware layout) to use for block 500, rather than creating a custom multiplier circuit that can't multiply by 0, +1, or -1.

Applicant submits that Office Action page 4 discussion regarding US 5,262,973 Figure 5 anticipating claim 1 rests solely on the "halt" signal applied to block 500 making the multiplier of block 500 "able" or "not able" to compute Z = X Y. Applicant further submits that the "halt" signal is a control signal for block 500. Applicant further submits that the language of amended claim 1 clearly differentiates between "not able" on the basis of a "halt" signal and "not able" regardless of control signals.

Re Claims 2-8, 10, and 12, pages 5-6 of Office Action

Pages 5-6 of the Office Action reject claims 2-8, 10, and 12, all of which are dependent on claim 1, as being anticipated by Figure 5 of Richardson. In each instance, rejection is

based on "multiplier-defined restricted set[s]" according to the interpretation of a "halt" signal defining a multiplier's ability or inability to compute a given product.

Applicant submits that the present amendments to claim 1 and its dependent claims clarify that external control signals do not define a multiplier's ability or inability to compute a given product in the present invention.

Accordingly, Applicant submits that claims 2-10 and 12 are not anticipated by Richardson's Figure 5, and requests withdrawal of the rejection under 35 U.S.C. 102(b).

Re Claims 13-24, 26, and 28-32, pages 7-8 of Office Action

Claim 13 and its dependent claims are analogous to claim 1 and its dependent claims except with both multiplier inputs subject to restrictions. In other words, the multiplier output is the product of two inputs only when each is from a strict subset of the set of all possible values. Referring to the example above, when X is one of a limited number of 16-bit twos' complement representations AND Y is one of a limited number of 18-bit twos' complement representations, Z is the product X Y. When either X or Y fails to be from the corresponding restricted set, Z is not the product X Y.

Office Action rejected claims 13-24, 26, and 28-32 under 35 U.S.C. 102 as anticipated by Figure 5 of Richardson for substantially the same reasons as rejection of claim 1 and its dependent claims under 35 U.S.C. 102.

Applicant has amended claim 13 and dependent claims to clarify that external control signals do not define a multiplier's ability or inability to compute a given product in the present invention.

Accordingly, Applicant submits that claims 13-24, 26, and 28-32 are not anticipated by Richardson's Figure 5, and requests withdrawal of the rejection under 35 U.S.C. 102(b).

The Rejections of Claims Under 35 USC SS 103

The Office Action rejected claims 9 and 25 under 35 U.S.C. 103(a) as "obvious over Richardson (U.S. 5,262,973) in view of Deutsch et al. (U.S. 4,031,377)."

Claim 9 is a dependent claim of machine claim 1, while claim 25 is an analogous dependent claim of method claim 17, which is itself a method claim similar to claim 1.

As noted above, Applicant has amended claim 1 to properly distinguish the present invention from the material in Richardson, in particular that in the present invention ability or inability of a multiplier to compute a product is not a function of multiplier control signals, whereas in Richardson ability or inability of the multiplier block 500 in Figure 5 to compute a product depends on a "halt" control signal. Applicant has also amended claim 17 similarly.

Applicant therefore submits that with the amendments to claims 1 and 17, claims 9 and 25 are not obvious under 35 U.S.C. 103(a) with respect to the combination of the Richardson and Deutsch et al. patents, and requests withdrawal of the rejections under 35 U.S.C. 103(a).

Comments on Prior Art Made of Record and Not Relied Upon

The Office Action included a list of 4 additional U.S. Patents not listed in the Applicant's IDS filing that were deemed relevant to the Applicant's pending application but not discussed in detail in the Office Action. Below Applicant includes a summary of each of the 4 prior art references and some comments on differences between the prior art and the present invention. The comments are in the same order as the list in the Office Action.

Comments on U.S. Patent 6,223,197 Issued to Kosugi

U.S. Patent 6,223,197 entitled "Constant multiplier, method and device for automatically providing constant multiplier and storage medium storing constant multiplier automatic providing program" and issued to K. Kosugi on April 24, 2001 discusses hardware multipliers intended for use in certain types of signal processing transforms, notably MPEG video. The patent discusses the motivation for a constant multiplier rather than a general multiplier in column 1, lines 39-59. Other aims of the patent are automated software design of constant multipliers, so that human designers do not have to undertake an expensive manual design in order to implement constant multipliers.

Applicant notes that in Kosugi and other prior art relating to constant multipliers, one multiplier input is implicitly restricted (by whatever reduced-cost computation structure is used) to being the constant while the other multiplier input is not. In the present invention, more than one first multiplier input is permitted (since the first multiplier-defined restricted set has more than one member), so there is at least one input which is neither a constant nor free to be any representation supported by its numeric format.

For instance, the first multiplier input could be a communications symbol from a 64-QAM alphabet in 16-bit two's complement representation. There are only 64 possible symbols, but 65536 representations. A first restricted set might contain at least the 64 representations corresponding to the 64 symbols, but not all 65536 representations.

Comments on U.S. Patent 6,629,120 Issued to Walster et al.

U.S. Patent 6,629,120 entitled "Method and apparatus for performaing mask-driven interval multiplication operation" and issued to G.W. Walster and D. Chiriaev on September 30, 2003 discusses multiplication using interval arithmetic. Applicant's understanding of Walster and Chiriaev's definition of interval arithmetic is that rather than a number one has an interval defined by two endpoints, which are numbers. "Multiplying" one interval by another interval produces a third interval whose endpoints are determined by the maximum and minimum products possible with numbers in the two input intervals.

Applicant submits that the present application deals with multiplication of numbers rather than intervals and so is unrelated to Walster and Chiriaev's patent. Insofar as the finite-precision number representations in the present invention represent intervals, all numbers in the corresponding interval are mapped to one number representation which may or may not admit well-defined interval endpoints such as half of the distance to adjacent exactly-represented numbers.

Comments on U.S. Patent 6,714,957 Issued to Lohman

U.S. Patent 6,714,957 entitled "System and method for efficient processing of denormal results as hardware exceptions" and issued to J.A. Lohman on March 30, 2005 discusses floating point multipliers. Floating point numbers are typically represented with some bits (say, 6 of them) representing an exponent and other bits (say, 9 of them) representing a mantissa. The actual number being represented is the mantissa multiplied by a number taken to the exponent (2-to-the-exponent, for instance). The number of bits allocated to the exponent determines a quantization of a large absolute range of number values, while the number of bits allocated to the mantissa determines a smaller quantization around each admissible exponent value. In other words, the exponent determines very large quantization steps, and the mantissa determines very small ones.

The "denormal" results, according to Lohman, occur when decimal (more generally, representation element) places appear in the mantissa rather than the exponent. A normal representation of the decimal number 0.2 would be 2.0 x 10^(-1), while a denormal representation would be 0.2 x 10^(0). The denormal results addressed by Lohman's patent occur when the exponent takes on its minimum value AND additional representation element (decimal, binary, et cetera) places appear in the mantissa, in other words, for very tiny results. Ostensibly these very tiny results appear somewhat rarely but do not require full floating point processing. Lohman's patent attempts to save some of the processing costs by identifying the presence of denormal results and using reduced-cost processing techniques thereon.

Applicant's pending application is not restricted to denormal floating point numbers or even to floating point numbers, though it could be used in multiplying denormal floating point numbers.

Comments on U.S. Patent 6,658,443 Issued to Walster

U.S. Patent 6,658,443 entitled "Method and apparatus for representing arithmetic intervals within a computer system" and issued to G.W. Walster on December 2, 2003 discusses multiplication of one interval defined by a pair of endpoint values by another interval defined by a pair of endpoint values.

Applicant has noted differences between multipliers according to the present invention and interval multipliers above in discussion related to U.S. Patent 6,629,120.

CONCLUSION

For all of the above reasons, the Applicant submits that the specification and the claims are now in proper form, and that the claims are all patentable over the prior art. Therefore, the Applicant submits that this application is now in condition for allowance, which action is respectfully solicited.

Conditional Request for Constructive Assistance

The Applicant has amended the specification and claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, the Applicant, an independent inventor and pro se filer, respectfully requests the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P SS 2173.02 and SS 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Very Respectfully,

Charles D. Murphy

Charles D. Murphy
601 Linden Place #210
Evanston, IL 60202
(847) 864-8514

Certificate of Mailing: I hereby certify that this correspondence, and attachments, if any, will be deposited with the United States Postal Service by Express Mail, postage prepaid, in an envelope addressed to "Mail Stop Non-Fee Amendments, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below.

November 10, 2004 Charles Douglas Murphy

Charles Douglas Murphy, Applicant